SINGLE-INDUCTOR QUADRUPLE-OUTPUT TFT LCD POWER SUPPLY

FEATURES

- **Main Output, V_{MAIN}**
  - **– Adjustable Voltage, 3.0 V to 5.6 V/25 mA**
  - **– Post-Regulated for Low Ripple (5mV_{PP})**
  - **– ±0.8% Typical Accuracy**
  - **– Efficiency up to 83%**
- **Positive Output, V_{GH}**
  - **– Adjustable Voltage up to 20 V/2 mA**
  - **– ±3% Typical Accuracy**
- **Negative Output, V_{GL}**
  - **– Adjustable Voltage down to -18 V/2 mA**
  - **– ±3% Typical Accuracy**
- **Auxiliary 1.8 V/3.3 V Linear Regulator**
- **Automatic or Programmable Power Sequencing**
- **Complete 1 mm Component Profile Solution**
- **2.5 V to 5.5 V Input Voltage Range**
- **Output Short Circuit Protected**
- **16-Pin QFN Package (3 × 3 × 0,9 mm)**

APPLICATIONS

- **Small Form Factor a-Si and LTPS TFT LCD**
- **Cell Phones, Smart Phones**
- **PDAs, Pocket PCs**
- **Portable DVD**
- **Digital-Still Cameras, Camcorders**
- **Handheld Instruments**
- **Portable GPS**
- **Car Navigation Systems**

DESCRIPTION

The TPS6512x DC-DC converter supplies all three voltages required by amorphous-silicon (a-Si) and low-temperature poly-silicon (LTPS) TFT-LCD displays. The compact layout of the TPS6512x uses a single inductor to generate independently-regulated positive and negative outputs. A free-running variable peak current PWM control scheme time-multiplexes the inductor between outputs. This control architecture operates at a pseudo-fixed-frequency to provide fast response to line and load transients while maintaining a relatively constant switching frequency and high efficiency over a wide range of input and output voltages. Due to the high switching frequency capability of the device, inexpensive and ultra-thin 8.2 or 10 µH inductors can be used.

The main output, V_{MAIN}, is post-regulated to provide a low-ripple source drive voltage for the LCD display. The auxiliary outputs generate a boosted output voltage, V_{GH}, up to 20 V, and a negative output voltage, V_{GL}, down to -18 V for the LCD gate drive. The device has internal current limiting for high reliability under fault conditions. Additionally, the device offers a fixed output linear regulator for the LCD logic circuitry.

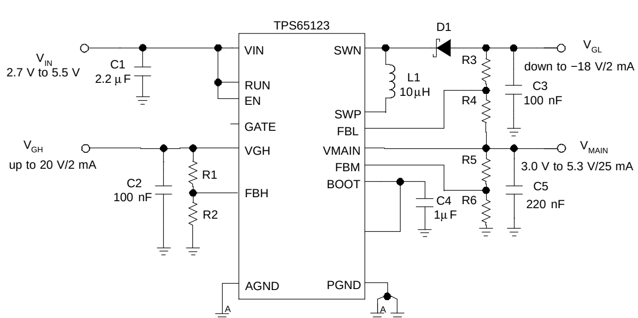


Figure 1. Typical Application

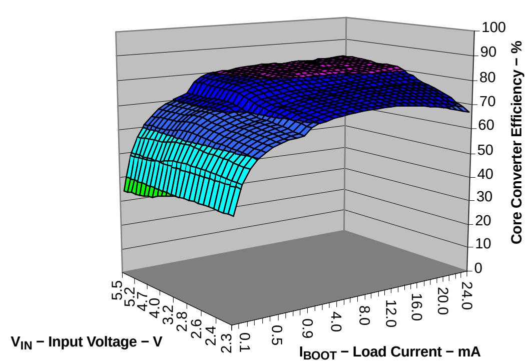


Figure 2. Core Converter Efficiency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	INTEGRATED LINEAR REGULATOR	POWER SEQUENCING	PACKAGE	PART NUMBER(1)	PACKAGE MARKING
-40 to 85°C	Fixed 3.3V output voltage	Automatic Power-Up/Down	3 × 3 QFN-16	TPS65120RGT	BKA
	Fixed 1.8V output voltage	Automatic Power-Up/Down	3 × 3 QFN-16	TPS65121RGT	BKB
	NO	Automatic Power-Up/Down	3 × 3 QFN-16	TPS65123RGT	BKC
	NO	Programmable Power-Up/Down	3 × 3 QFN-16	TPS65124RGT	BKD

(1) The xyz package is available in tape and reel. Add R suffix (xyzR) to order quantities of TBD parts. Add T suffix (xyzT) to order quantities of 250 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Input voltage(2)	VIN	-0.3 V to +6 V
	SWN	V_{IN} - 24 V to V_{IN} +0.3 V
	SWP	- 0.3 V to +23 V
Voltage(2)	VGH	- 0.3 V to +21 V
	VMAIN, LDOIN, LDOOUT, ENVGL, ENVGH	- 0.3 V to +6 V
	BOOT	- 0.3 V to +6.2 V
Input voltage at GATE, EN, RUN (2)		-0.3 V to V_{IN} + 0.3 V
Power dissipation		Internally limited
Operating temperature range		-40°C to 85°C
Maximum operating junction temperature, T_J(max)		135°C
Storage temperature range		65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C
RGT	68°C/W	15mW/°C

(1) Maximum power dissipation is a function of T_J(max), θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max)-T_A]/\ \theta_{JA}$.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6 V, EN = RUN = V_{IN}, L = 10 µH, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONVERTER STAGE						
V_{IN}	Input voltage for full load operation	R_{L_MAIN} ≥ 330 Ω at V_{MAIN} = 5 V, R_{L_VGH} ≥ 12 kΩ at V_{GH} = 12 V, R_{L_VGL} ≥ 12 kΩ at V_{GL} = -12 V, V_{LDOIN} = GND, T_A = -40°C to 85°C	2.7		5.5	V
	Minimum input voltage for start-up	R_{L_MAIN} ≥ 660 Ω at V_{MAIN} = 5 V, R_{L_VGH} ≥ 24 kΩ at V_{GH} = 12 V, R_{L_VGL} ≥ 24 kΩ at V_{GL} = -12 V, V_{LDOIN} = GND, T_A = -20°C to 85°C	2.5			V
f	Switching frequency	R_{L_MAIN} = 250 Ω at V_{MAIN} = 5 V, V_{LDOIN} = ENVGH = ENVGL = GND		4.0		MHz
P_{GH}	Output power on V_{GH}	V_{IN} ≥ 2.7 V	35			mW
		V_{IN} ≥ 2.5 V	15			
P_{GL}	Output power on V_{GL}	V_{IN} ≥ 2.7 V	35			mW
		V_{IN} ≥ 2.5 V	15			
P_{TOT}	Total output power on V_{BOOT} + V_{GH} + V_{GL}	V_{IN} ≥ 2.5 V	60			mW
		V_{IN} ≥ 2.7 V	120			
		V_{IN} ≥ 3 V	150			
		V_{IN} ≥ 4.5 V	250			
η	Power efficiency	V_{MAIN} = 5.0 V, I_{BOOT} = 20 mA, V_{GH} = 15 V, V_{GL} = -10 V, I_{GH} = I_{GL} = 100 µA, V_{LDOIN} = GND		83%		
I_{LIM}	P-MOS1 current limit	2.7 V ≤ V_{IN} ≤ 5.5 V		150	200	mA
$I_{START-UP}$	P-MOS1 start-up current limit	2.7 V ≤ V_{IN} ≤ 5.5 V		65		mA
$r_{DS(ON)}$	P-MOS1 switch on-resistance	V_{IN} = V_{GS} = 3.6 V		2.5	4.3	Ω
		V_{IN} = V_{GS} = 2.5 V		3.8	6.9	
	N-MOS1 switch on-resistance	V_{BOOT} = V_{GS} = 3.7 V		1.9	3.5	Ω
		V_{BOOT} = V_{GS} = 5 V		1.4	2.3	
	P-MOS1 leakage current	V_{DS} = 6 V, T_A = 25°C		0.01		µA
	N-MOS1 leakage current			0.01		
	N-MOS2 + P-MOS2 forward voltage drop	V_{GS} = V_{BOOT} = 5.5 V, V_{SWP} = 2 V, I_{BOOT} = I_D = 50 mA		400	600	mV
	N-MOS3 + D1 forward voltage drop	V_{GS} = V_{BOOT} = 5.5 V, V_{SWP} = 2 V, I_{GH} = I_D = 50 mA		900	1100	mV
CONVERTER SUPPLY CURRENT						
I_Q	Quiescent current into VIN	I_{MAIN} = I_{GH} = I_{GL} = 0 mA, V_{GH} = +15 V, V_{GL} = -15 V, V_{MAIN} = 5 V, V_{FBH} = V_{FBM} = +1.5 V, V_{FBL} = -0.2 V, V_{BOOT} = 5.25 V, V_{LDOIN} = GND, EN = RUN = V_{IN}, T_A = 25°C		140	170	µA
	Quiescent current into BOOT			30	60	
	Quiescent current into VGH			0.1	1	
I_{SD}	Shutdown current	T_A = 25°C		0.1	1	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6 V, EN = RUN = V_{IN}, L = 10 µH, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAIN OUTPUT						
V_{MAIN}	Main output voltage range		3.0		5.6	V
I_{MAIN}	Maximum main output current	$V_{MAIN} \le$ 5.3 V	25			mA
		$V_{MAIN} \ge$ 5.3 V	7.5			
V_{FBM}	Feedback regulation voltage	2.7 V ≤ $V_{IN} \le$ 5.5 V, 100 µA ≤ $I_{MAIN} \le$ 25 mA, T_A = -20°C to 50°C	1.203	1.213	1.223	V
		2.7 V ≤ $V_{IN} \le$ 5.5 V, 0 mA ≤ $I_{MAIN} \le$ 25 mA	1.195	1.213	1.231	V
I_{FBM}	Feedback input bias current	V_{FBM}= V_{REF}		0.01	0.1	µA
	Load regulation	I_{MAIN} = 0 to 25 mA, V_{MAIN} = 5 V		0.006		%/mA
	Minimum dropout voltage	I_{MAIN} = 10 mA		130		mV
	Main output voltage ripple	I_{MAIN} = 10 mA		5		mV_{P-P}
I_{SC_MAIN}	Short-circuit current limit	V_{BOOT} = 5.5 V			50	mA
R_{DIS_VMAIN}	Discharge resistor for power-down sequence			10		kΩ
VGH OUTPUT						
V_{GH}	V_{GH} output voltage range		V_{IN} + 0.5		20	V
I_{GH}	Maximum DC output current				6	mA
	V_{GH} precharge resistor			1		kΩ
V_{FBH}	Feedback regulation voltage	2.7 V ≤ $V_{IN} \le$ 5.5 V, 0 mA ≤ $I_{GH} \le$ 2 mA	1.177	1.213	1.249	V
I_{FBH}	Feedback input bias current	V_{FBH} = 0 V		0.01	0.1	µA
	Load regulation	I_{GH} = 0 to 2 mA, V_{GH} = 15 V		-0.11		%/mA
	Line regulation	V_{IN} = 2.7 V to 5.5 V, I_{GH} = 100 µA		0.01		%/V
	V_{GH} output voltage ripple	200 µA load, V_{GH} = 15 V, C_{OUT} = 220 nF, C_{FF} = 10 pF		20		mV
R_{DIS_VGH}	Discharge resistor for power-down sequence			10		kΩ
VGL OUTPUT						
V_{GL}	V_{GL} Output voltage range		-18		-2.5	V
I_{GL}	Maximum DC output current				6	mA
V_{FBL}	Feedback regulation voltage	2.7 V ≤ $V_{IN} \le$ 5.5 V, 0 mA ≤ $I_{GL} \le$ 2 mA	-0.036	0	0.036	V
I_{FBL}	Feedback input bias current	V_{FBL} = 0 V		0.01	0.1	µA
	Load regulation	I_{GL} = 0 to 2 mA, V_{GL} = -15 V		0.13		%/mA
	Line regulation	V_{IN} = 2.7 V to 5.5 V, I_{GL} = 100 µA		0.1		%/V
	V_{GL} output voltage ripple	200 µA load, V_{GL} = -15 V, C_{OUT} = 220 nF		20		mV

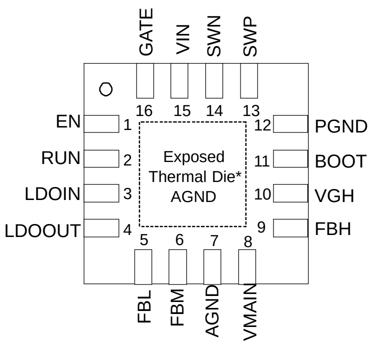
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6 V, EN = RUN = V_{IN}, L = 10 µH, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

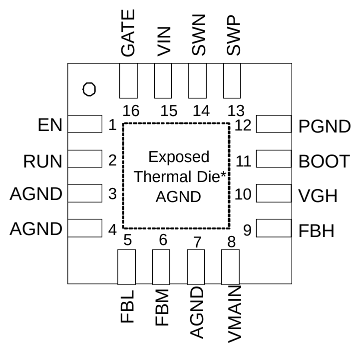
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINEAR REGULATOR STAGE - AUXILIARY OUTPUT						
V_{LDOIN}	Input voltage range		2.5		5.8	V
V_{LDOOUT}	Output voltage range		1.8		V_{LDOIN} -0.5	V
I_{LDOOUT}	Maximum output current		20			mA
I_{SC_LDO}	Short-circuit current limit	V_{LDOOUT} = 0 V			50	mA
	Minimum dropout voltage	I_{LDOOUT} = 10 mA			400	mV
	Total accuracy	2.5 V ≤ V_{LDOIN} ≤ 5.5 V, 0 mA ≤ I_{LDOOUT} ≤ 20 mA			±3%	
	Load regulation	I_{LDOOUT} = 0 to 20 mA		0.006		%/mA
	Line regulation	V_{LDOIN} = V_{LDOOUT} + 0.5 V (min 2.5 V) to 5.5 V, I_{LDOOUT} = 20 mA		0.013		%/V
I_{Q_LDO}	Linear regulator quiescent current	V_{LDOIN} = V_{LDOOUT} + 0.4 V (min 2.5 V), T_A = 25°C		11	20	µA
I_{SD_LDO}	Linear regulator shutdown current	GATE = VIN		0.2	1	µA
GATE DRIVER						
	Gate output pull-down resistance	V_{GATE} < 500 mV		100		kΩ
	Gate output pull-up resistance			100		kΩ
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	V
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.15	2.3	V
LOGIC SIGNALS EN, RUN, ENVGL, ENVGH						
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	V
I_{LKG}	Logic input leakage current	ENVGL, ENVGH = V_{IN} or GND (TPS65124)		0.01	0.1	µA
		EN, RUN = V_{IN}		0.01	0.1	µA
	EN, RUN pin pull-down resistance	EN, RUN ≤ 0.4 v		100		kΩ

PIN ASSIGNMENTS

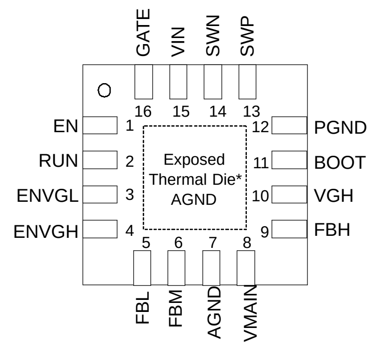
TPS65120/1/2
(TOP VIEW)



TPS65123
(TOP VIEW)



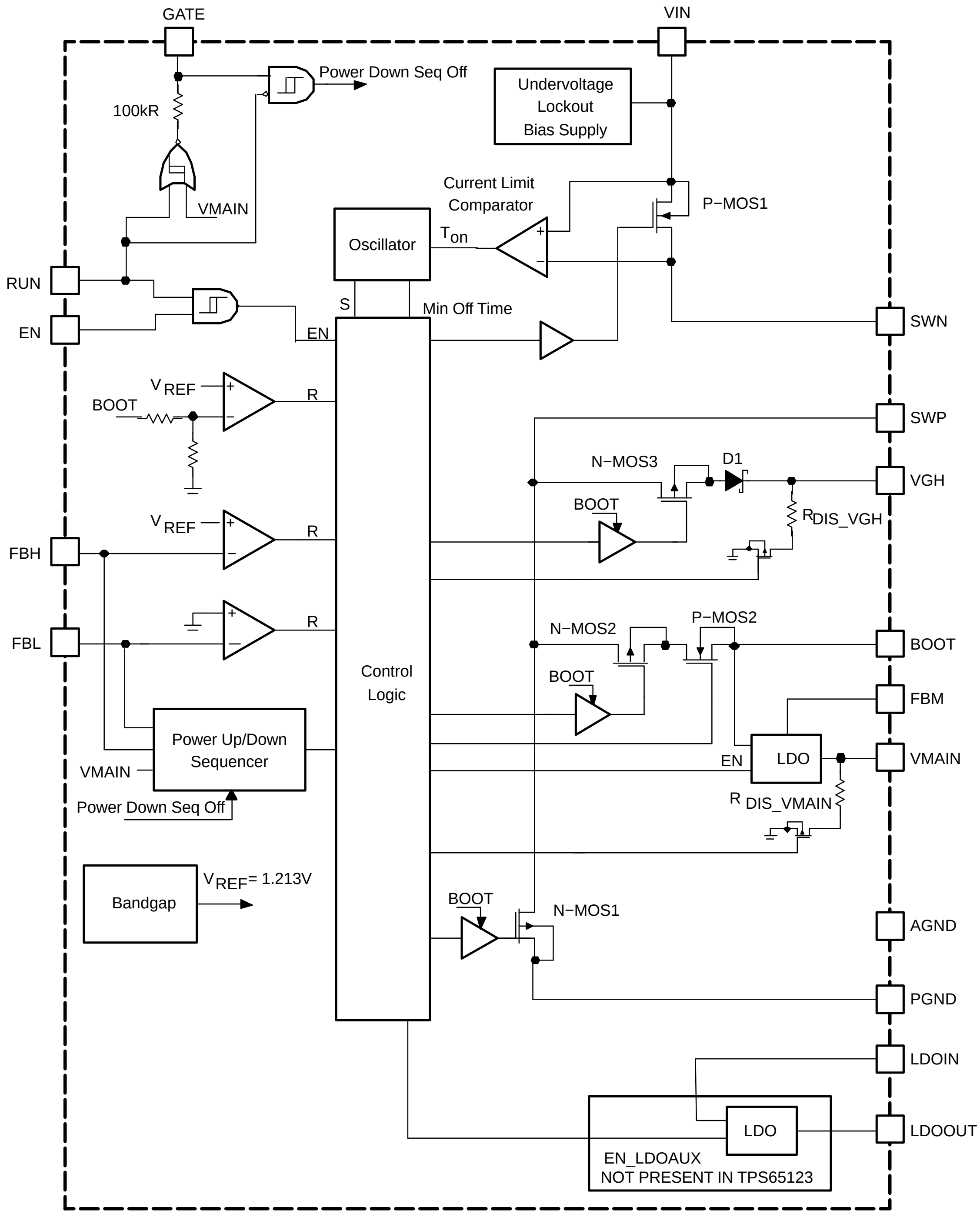
TPS65124
(TOP VIEW)



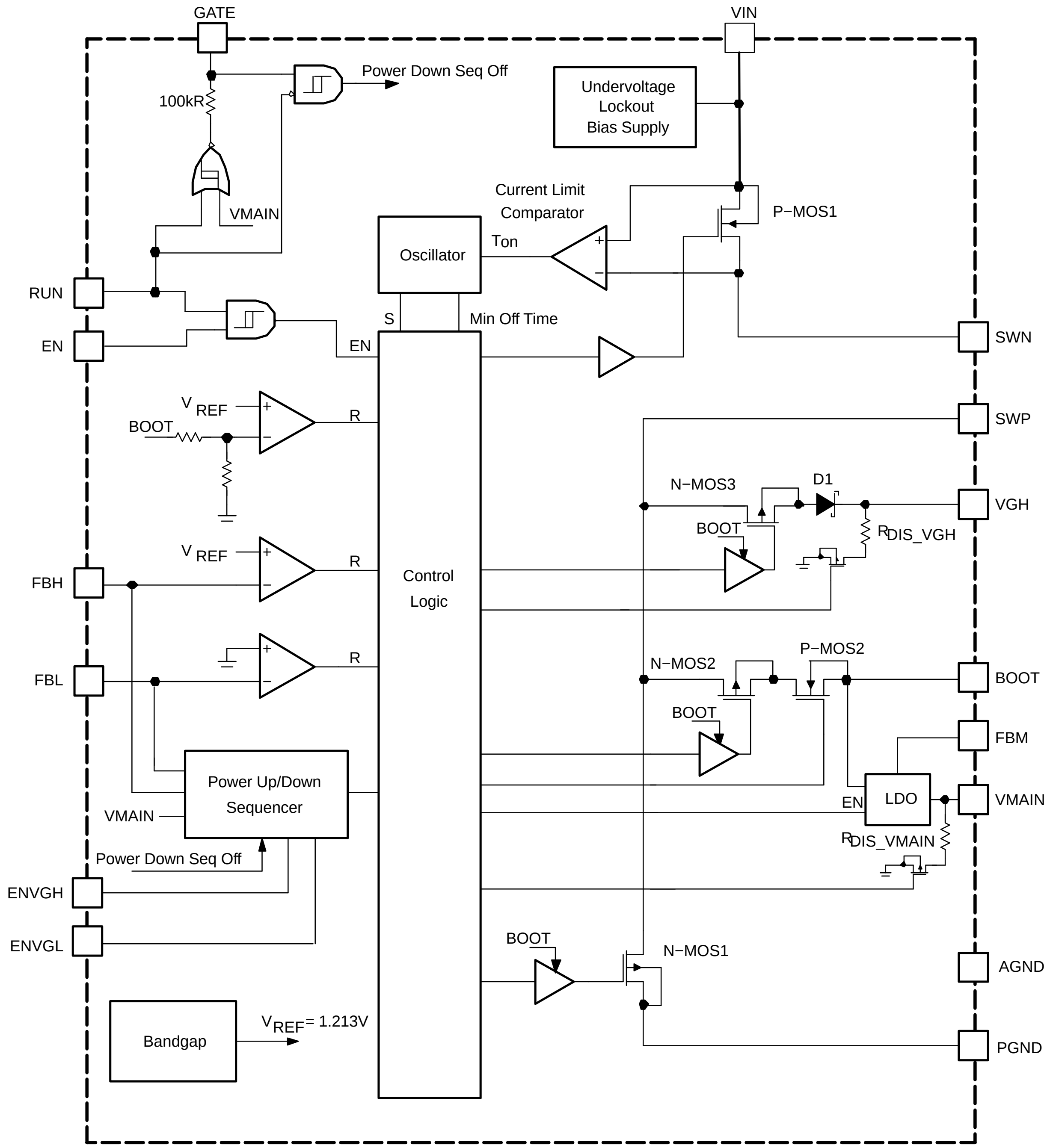
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	15	I	This is the input voltage pin of the device.
GATE	16	I/O	This pin can either be the gate driver output to an external small P-Channel MOSFET (see application section), or an active high control input. Pulling GATE above the 1.4 V logic-high level and RUN to a logic-low level disables the integrated active power-down sequencing.
RUN	2	I	RUN controls the external P-Channel MOSFET. This pin must be terminated and not be left floating. Forcing this pin to a logic-high level turns on the external MOSFET switch.
EN	1	I	This is the enable pin of the multiple-output dc-to-dc converter. This pin must be terminated and not be left floating. A simultaneous logic-high level on EN and RUN enables the converter and a logic-low shuts down the device.
SWN	14	I/O	Connect the inductor to this pin. This pin is connected to the source of the high-side MOSFET switch.
SWP	13	I/O	Connect the inductor to this pin. This pin is connected to the drain of the low-side MOSFET switch.
PGND	12	O	Power ground. Connect to AGND underneath the IC.
VGH	10	O	Positive output
BOOT	11	O	Provides a bootstrapped supply for the rectifier MOSFET driver, enabling the gate of the MOSFET to be driven above the output voltage.
VMAIN	8	I	Main output
FBH	9	I	Feedback pin for the positive output voltage divider. Regulates to 1.213 V nominal.
FBL	5	I	Feedback pin for the negative output voltage divider. Regulates to 0 V nominal. Connect feedback resistor divider between VGL and main output.
FBM	6	I	Feedback pin for the main output voltage divider. Regulates to 1.213V nominal.
AGND	7, 3, 4		Analog ground. Connect to power ground (PGND) underneath IC. Pins 3 and 4 are only used for AGND in TPS65123.
LDOIN	3	I	Auxiliary linear regulator input. If this pin is connected to GND, the voltage regulator is disabled (TPS65120/1/2). The low-dropout series-pass regulator (LDO) is enabled according to the GATE signal timing.
LDOOUT	4	O	Auxiliary linear regulator output (TPS65120/1/2).
ENVGL	3	I	Enable pin for negative output (TPS65124). This pin should be terminated and not be left floating.
ENVGH	4	I	Enable pin for positive output (TPS65124). This pin should be terminated and not be left floating.

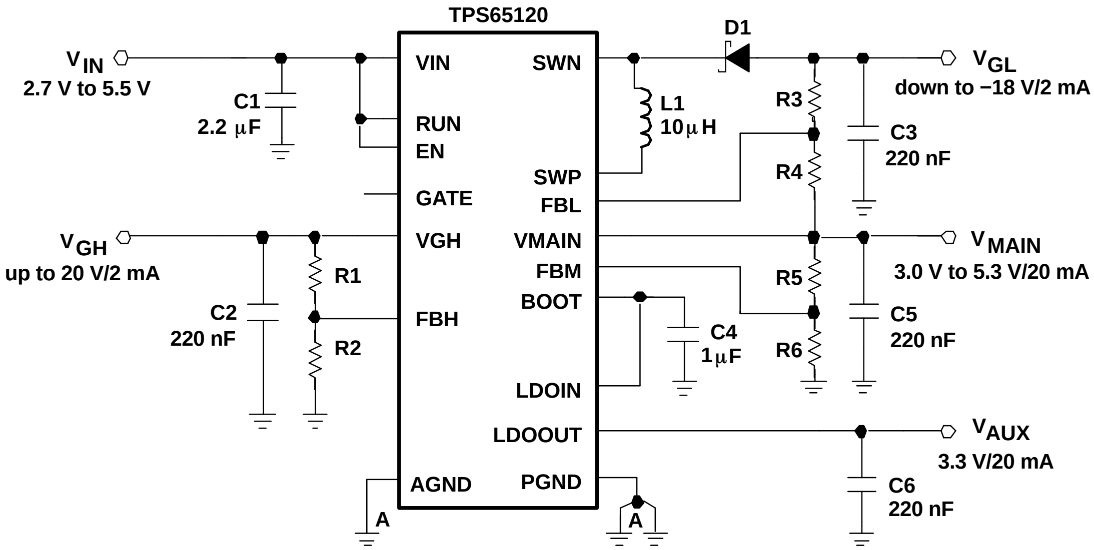
FUNCTIONAL BLOCK DIAGRAM - TPS65120/1/2/3



FUNCTIONAL BLOCK DIAGRAM - TPS65124



PARAMETER MEASUREMENT INFORMATION



List of Components:
U_1 = TPS6512x
L_1 = EPCOS SIMID1812-C
D_1 = ZETEX ZUMD54C
C_X = X5R/X7R

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Core converter efficiency	vs Load current	3
		vs Input voltage	4
	Main output efficiency	vs Load current	5
		vs Input voltage	6
V_{MAIN}	Output ripple voltage		7
	DC output voltage	vs Load current	8
	Load transient response		9
V_{GH}, V_{GL}	Positive, negative output ripple voltage		10, 11
V_{GH}	DC output voltage	vs Load current	12
V_{GL}	DC output voltage	vs Load current	13
f_s	Switching frequency	vs Load current	14
I_Q	No load quiescent current	vs Input voltage	15
	Power-Up Sequencing (TPS65120)		16
	Power-Down Sequencing (TPS65120)		17

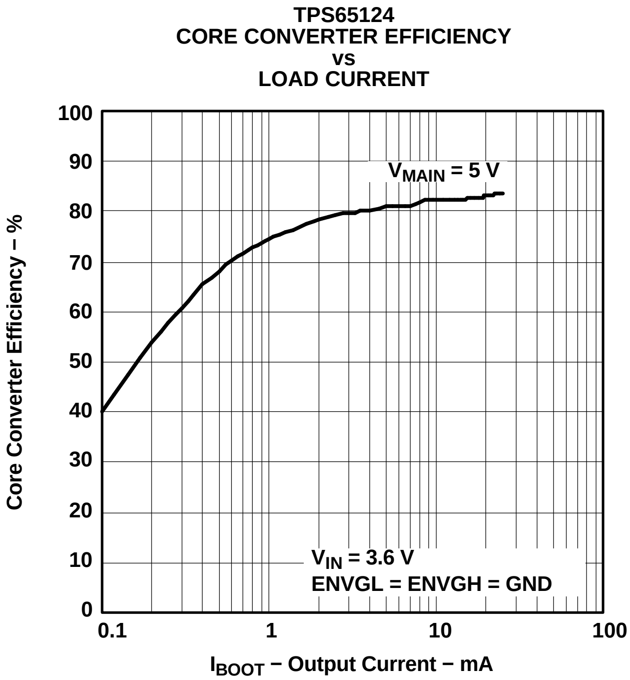


Figure 3.

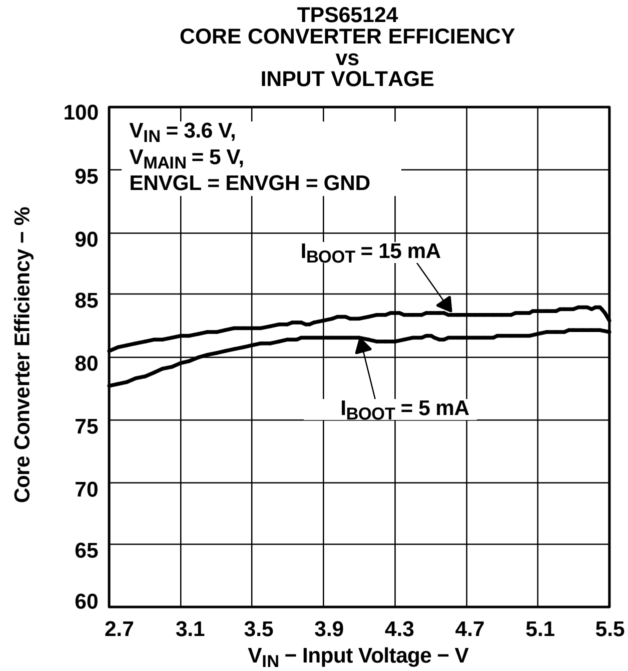


Figure 4.

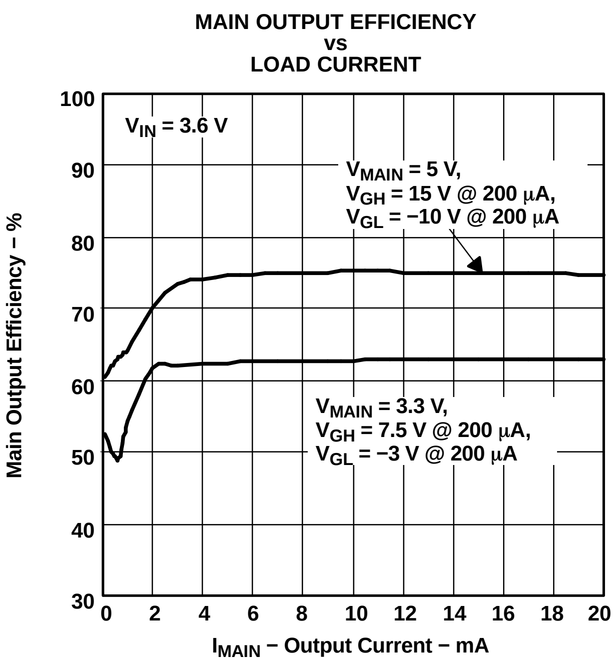


Figure 5.

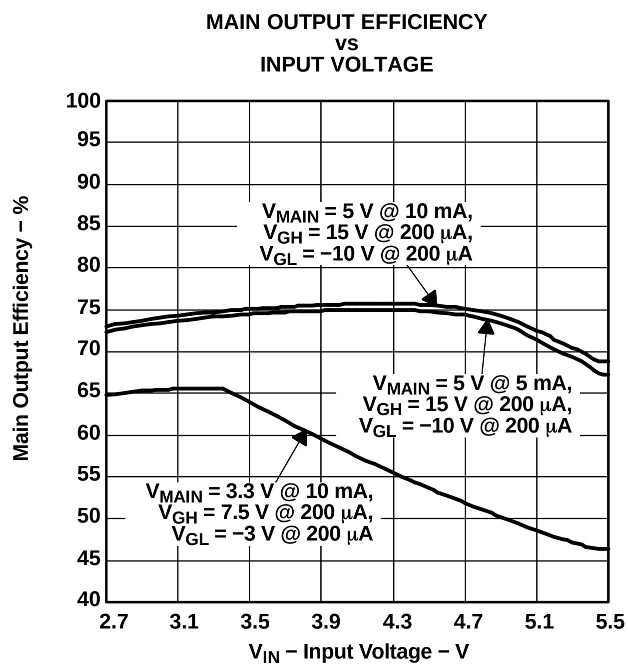


Figure 6.

MAIN OUTPUT RIPPLE VOLTAGE

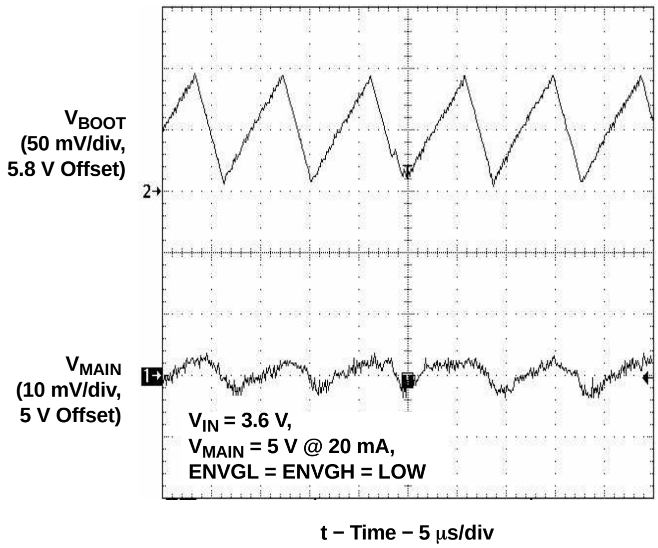


Figure 7.

MAIN DC OUTPUT VOLTAGE
vs
LOAD CURRENT

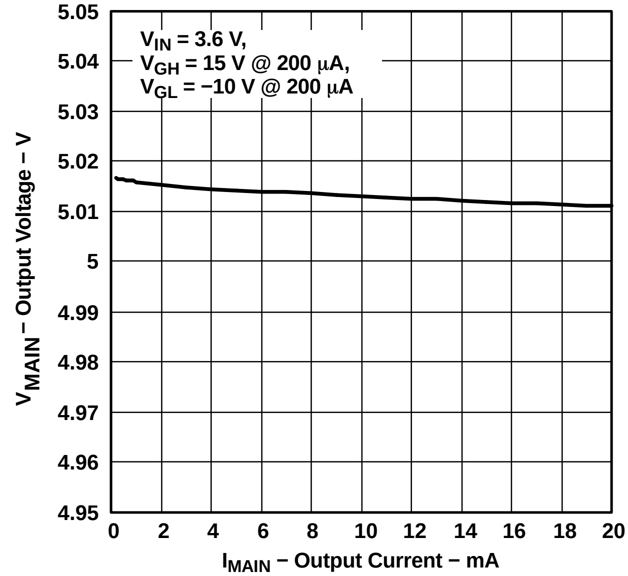


Figure 8.

MAIN OUTPUT LOAD
TRANSIENT RESPONSE

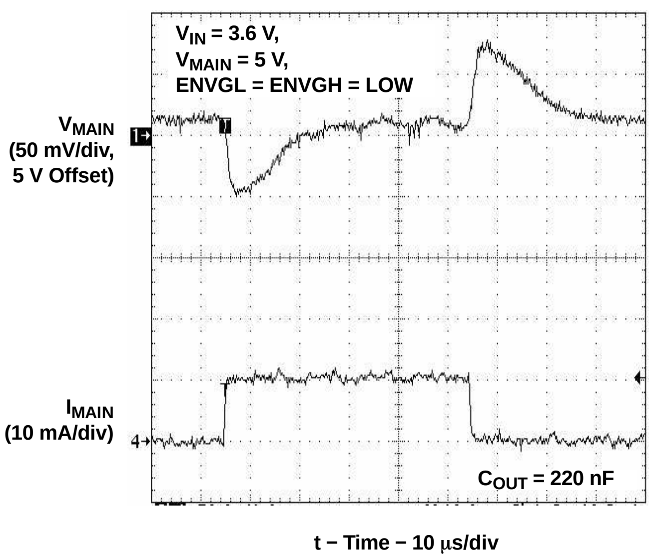


Figure 9.

POSITIVE, NEGATIVE OUTPUT RIPPLE

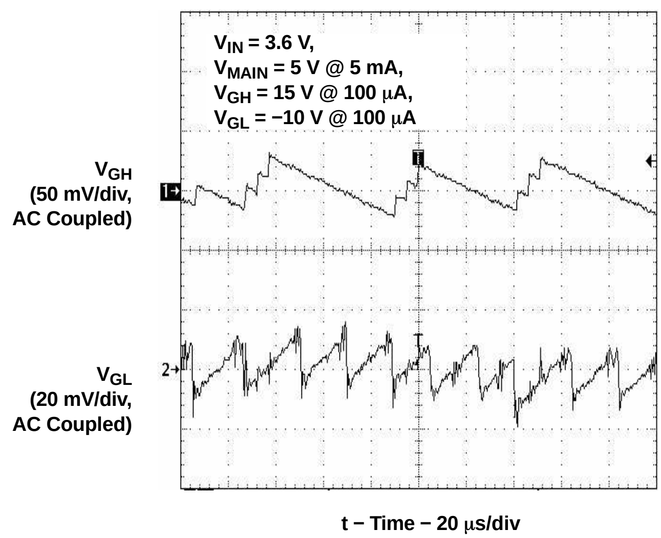


Figure 10.

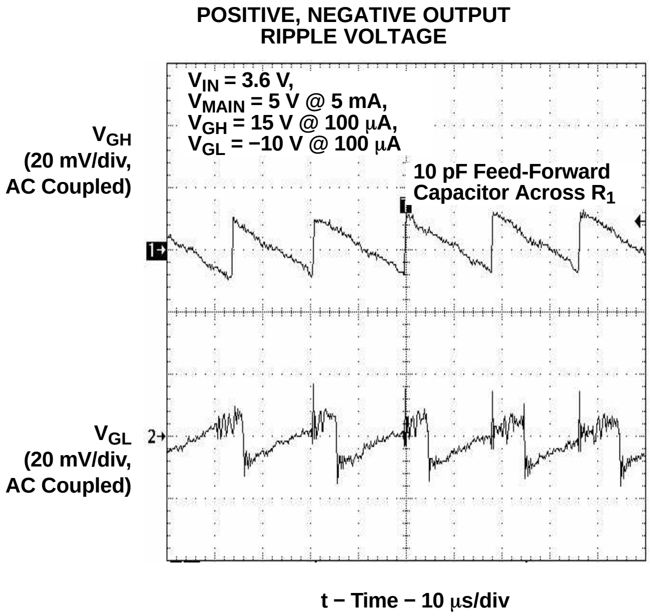


Figure 11.

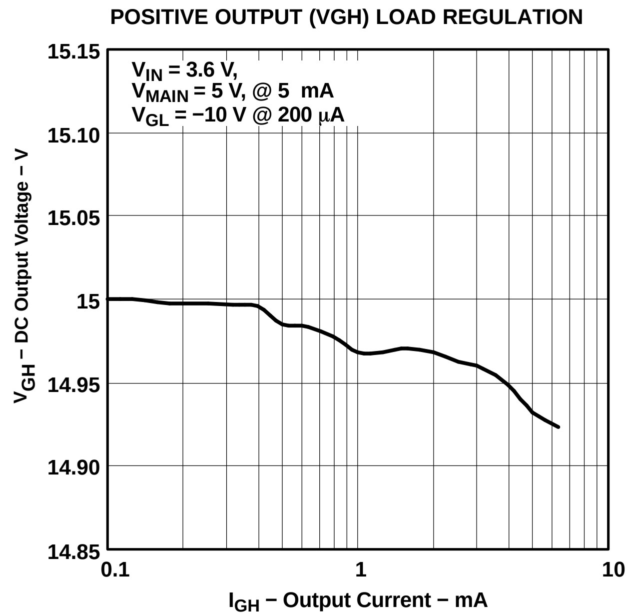


Figure 12.

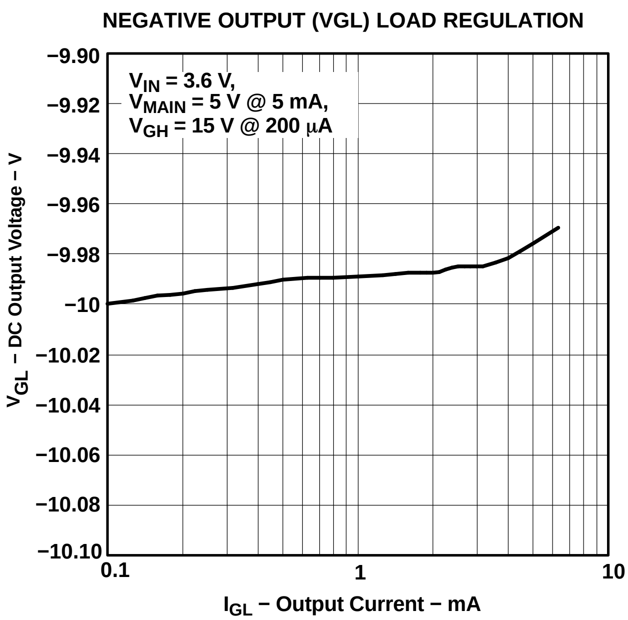


Figure 13.

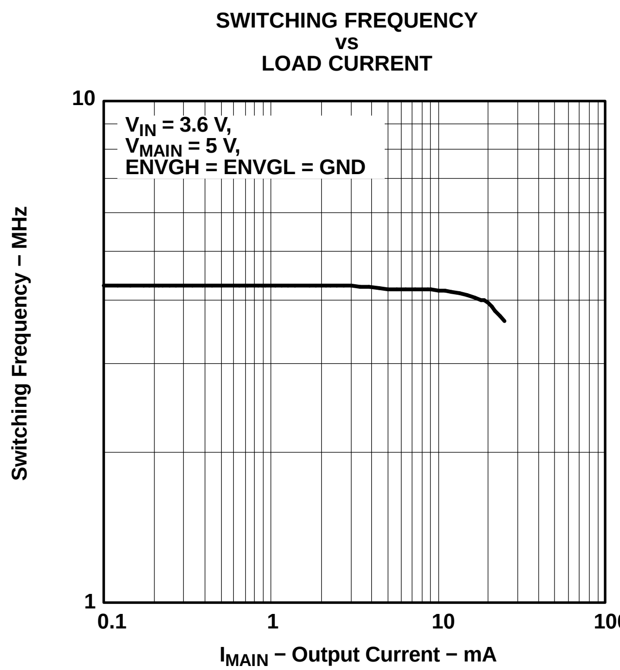


Figure 14.

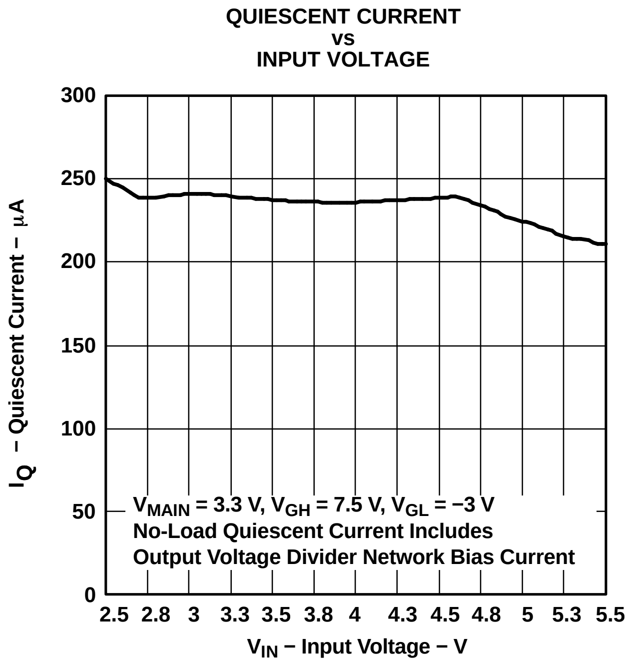


Figure 15.

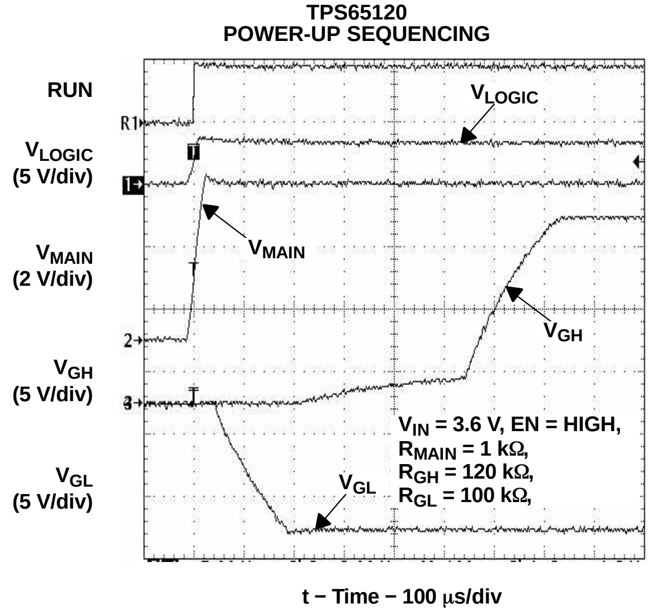


Figure 16.

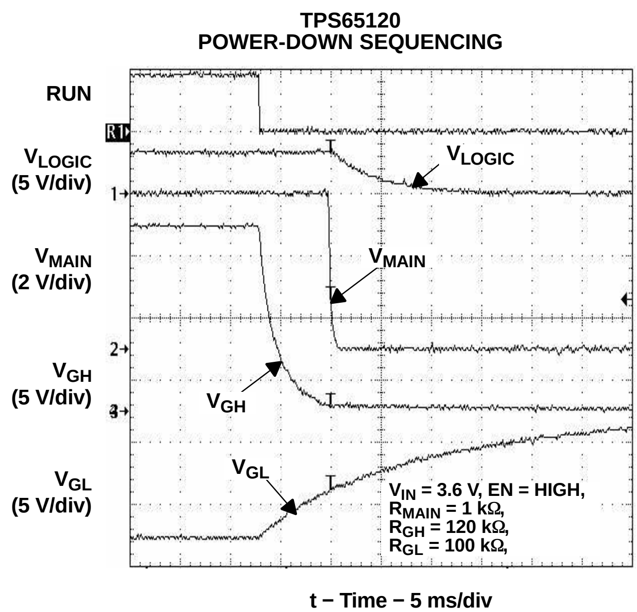


Figure 17.

DETAILED DESCRIPTION

The standard application circuit (Figure 1) of the TPS65120 is a complete power supply for TFT LCD displays. The circuit generates four independent supplies for the source driver (V_{MAIN}), the gate drivers (V_{GH}, V_{GL}) and a logic supply for the timing controller. The input voltage range is from 2.5 V to 5.5 V.

The TPS65120/1/2 contains a high-performance switching regulator and two low-dropout linear regulators (LDOs). One of the LDOs generates V_{MAIN} and the other powers the logic inside the panel. The TPS65123 includes only one linear regulator to provide the main output with low ripple voltage and can be set from 3.0 V to 5.3 V with an external resistor voltage divider. The TPS65124 integrates programmable power sequencing for highest flexibility.

OPERATION

The TPS6512x generates both positive and negative supply voltages using a single inductor. It alternates between acting as a step-up converter and an inverting converter on a cycle-by-cycle basis. All output voltages are independently regulated.

A free-running, variable-peak-current PWM control scheme is used to time-multiplex the inductor between BOOT, V_{GH}, and V_{GL} outputs. This inherently-stable control architecture operates at a pseudo fixed frequency, providing fast response to line and load transients while maintaining a relatively constant switching frequency and high efficiency over a wide range of input and output voltages.

During the first cycle of operation, internal switches N-MOS1 and P-MOS1 are turned on. SWN connects to VIN, SWP pulls to ground and the inductor current rises. Once the inductor current reaches the DC current limit (I_{LIM}) of 150 mA (typ) the internal control logic can either turn off N-MOS1 or P-MOS1 to service the requesting output. Depending on the required output power, the converter starts another cycle or enters a pulse-skipping modulation scheme to increase efficiency under light loads. The current into the SWN pin measures the inductor current. The TPS6512x controls the inductor current to regulate BOOT, V_{GH}, and V_{GL} output voltages.

To achieve low ripple voltage and high accuracy, the main output (V_{MAIN}) is post-regulated by an integrated LDO. This LDO regulator regulates energy from the BOOT output down to 5.3 V (max). To achieve the highest efficiency, the BOOT voltage is regulated to minimize the dropout voltage across the LDO to approximately V_{MAIN} + 0.5 V.

In addition, the VMAIN, VGH, VGL outputs are monitored for fault conditions that last longer than the fault-timer period of 100 µs (typ). The device goes into a latched shutdown state in case of a fault condition.

Soft Start

The TPS6512x has an internal soft-start circuit that limits the inrush current during startup. This prevents possible voltage drops of the input voltage in case the battery or a high impedance power source is connected to the input of the device.

The device powers up by precharging the BOOT output capacitor to VIN. During the precharge phase, the current through the rectifying switch N-MOS2 is limited. This also limits the output current under short-circuit conditions on the BOOT output. To ensure proper startup of the device, the BOOT output must be left unloaded during the precharge phase.

After the precharge phase, the converter operates with an $I_{START-UP}$ current limit of 65 mA (typ), then increases gradually to the full current limit of 150 mA (typ).

Undervoltage Lockout

To ensure that the input voltage is high enough for reliable operation, the TPS6512x includes an under-voltage lockout (UVLO) circuit. The UVLO threshold at the VIN pin is 2.15 V (typ) falling and 2.25 V (typ) rising. The 100 mV (typ) hysteresis prevents supply transients from causing restarts.

Once the input voltage exceeds the UVLO rising threshold, the controller can enable the reference voltage and precharges BOOT. When the input voltage falls below the UVLO falling threshold, the controller turns off the reference and all the regulator outputs, and pulls GATE high with an internal 100 kΩ resistor to turn off P1 (Figure 18).

DETAILED DESCRIPTION (continued)

Enable and Power Sequencing (TPS65120/1/2/3)

To correctly power up most TFT panels, the gate-drive supplies must be sequenced such that the negative supply (V_{GL}) powers up before the positive supply (V_{GH}). The TPS65120/1/2/3 controls this sequence through an enable pin.

Once RUN is high, the TPS65120/1/2/3 turns on the external P-channel MOSFET P1 (see Figure 18) by pulling GATE low. GATE is pulled down with a 100 kΩ resistor. The DC/DC converter then starts, enabling the BOOT output.

Pulling the enable pin (EN) high enables the MAIN output. When the output voltage V_{MAIN} has reached 90% of its nominal value, the negative output enables. V_{GH} is delayed until the negative voltage has reached 90% of its nominal value.

Pulling the RUN pin low shuts down the device. Power-down sequencing starts by switching off V_{GH} and V_{GL}.

The V_{GH} output capacitor is actively discharged by an internal resistor while V_{GL} is only discharged by its feedback voltage divider. The required time to discharge the output capacitor at V_{GL} output depends on the load current. Once V_{FBL} has reached 1.2 V (typ) the main output is turned off followed by the output voltage V_{LOGIC}. This sequence is shown in Figure 19.

When no power sequencing is required on the digital supply voltage (V_{LOGIC}), tie EN and RUN signals together and GATE can be connected to a logic-high level to disable the power-down sequencer. Each output turns off depending upon load current and output capacitance.

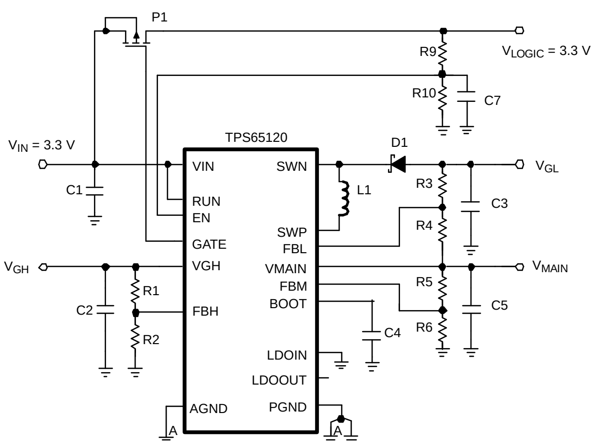


Figure 18. Power Sequencing on Digital Supply Voltage, V_{LOGIC}

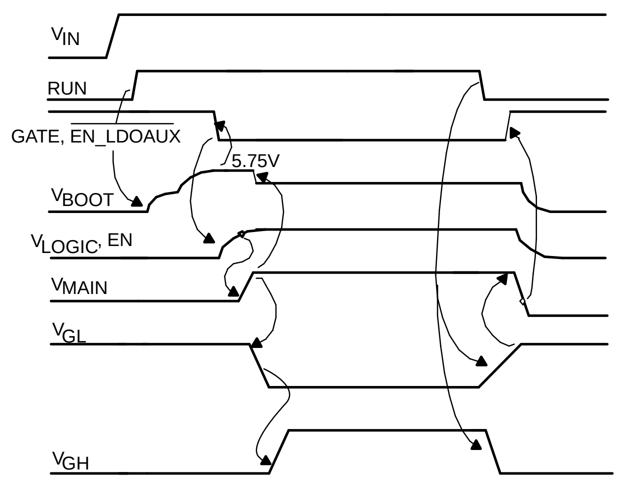


Figure 19. TPS65120/1/2/3 Power Sequence

DETAILED DESCRIPTION (continued)

Enable and Power Sequencing (TPS65124)

The TPS65124 controls the power sequencing of V_{LOGIC}, V_{MAIN}, V_{GH} and V_{GL} with four separate enable pins. These pins must be terminated and not be left floating to prevent instability.

Once RUN is pulled high and the input voltage on VIN exceeds the rising input UVLO threshold, the reference is turned on and the external P-channel MOSFET P1 (see Figure 20) is switched on by pulling GATE low. The GATE is pulled down with a 100 kΩ resistor. The DC/DC converter then starts up, enabling the BOOT output.

Pulling enable pin high (EN) powers on the MAIN output. This power sequencing must occur before the gate voltages are enabled. Conversely V_{GL} and V_{GH} output voltages must be turned off by pulling ENVGL and ENVGH inputs to ground before the MAIN output is switch off.

To clamp the V_{GL}output near zero when the MAIN output is still on, an external diode (D2) can be used. In some applications this diode may already be implemented in the display.

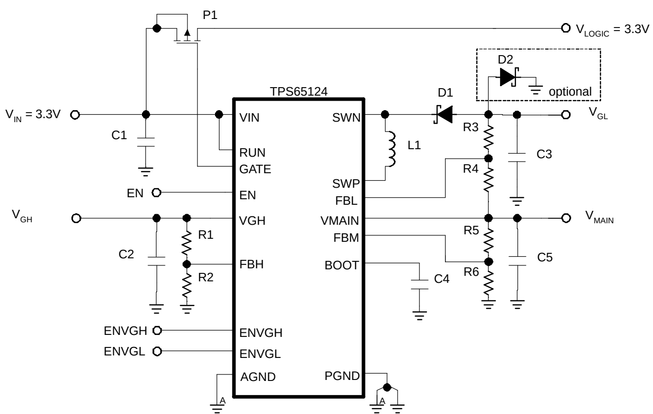


Figure 20. Power Sequencing on Digital Supply Voltage, V_{LOGIC}

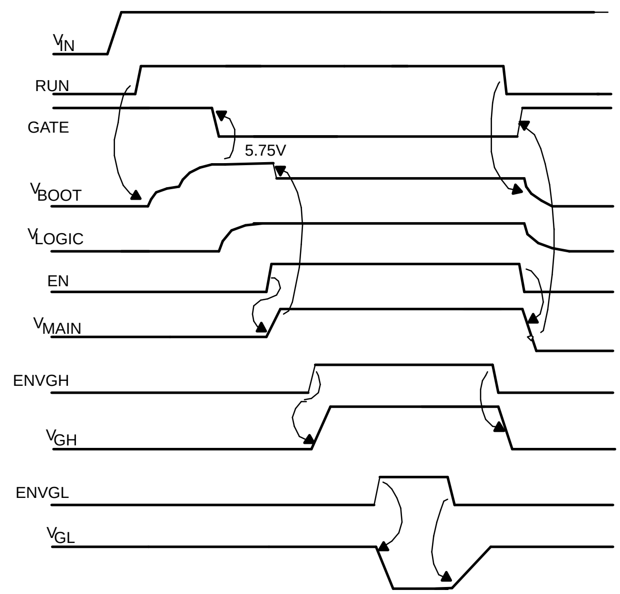


Figure 21. TPS65124 Programmable Power Sequence

Fault Protection

All TPS6512x outputs are protected against a short circuit to ground. During steady-state operation, if the output V_{MAIN}, V_{GH} or V_{GL} falls below its fault detection threshold the device simultaneously turns off all three outputs. Once V_{MAIN} comes down to 700 mV typ, the GATE output is pulled to V_{IN}, the auxiliary LDO (TPS65120/1/2) is disabled and the device enters a shutdown state.

The auxiliary LDO present in TPS65120/1/2 has an integrated current foldback circuit for reliable short-circuit protection.

The device can be enabled again by toggling the enable pins (RUN, EN) below 0.4 V or by cycling the input voltage below the UVLO falling threshold (2.15 V typ).

APPLICATION INFORMATION

OUTPUT POWER CAPABILITY

The first step in the design procedure is to calculate the maximum output current for each output under certain input and output voltage conditions. The TPS6512x uses time-multiplex operation to share the inductive storage element between BOOT, VGH and VGL outputs. To avoid complex calculations it is recommended to use the specified output-power data from the electrical characteristics table to determine the maximum output-power capability.

The following example shows how to proceed for given requirements:

- Input Voltage = 3.0 V
- MAIN Output = 5.0 V @ 10 mA
- VGH output = 12 V @ 500 µA
- VGL output = -12 V @ 300 µA

1. Calculate Maximum Output Power on VGH Output

$$P_{GH} = V_{GH} \times I_{GH}$$

2. Calculate Maximum Output Power on VGL Output

$$P_{GL} = \left|V_{GL}\right| \times I_{GL}$$

3. Calculate Maximum Output Power on BOOT Output

$$P_{BOOT} = P_{MAIN} \times \eta_{LDO\_MAIN} \approx \frac{V_{MAIN}^{2}}{V_{MAIN} + 0.5} \times I_{MAIN} \quad \text{for } V_{IN} < V_{MAIN} + 0.5$$

$$P_{BOOT} = P_{MAIN} \times \eta_{LDO\_MAIN} \approx \frac{V_{MAIN}^{2}}{V_{IN}} \times I_{MAIN} \quad \text{for } V_{IN} > V_{MAIN}$$

4. Maximum Output Power Verification

The electrical characteristics table states that for V_{IN} > 3.0 V, the maximum power on VGH and VGL outputs must be lower than 35 mW each. Furthermore, the total output power (P_{BOOT} + P_{GH} + P_{GL}) must be lower than 150 mW.

In our design example, P_{GH} = 6 mW, P_{GL} = 3.6 mW, and P_{BOOT} = 55 mW. Since these numbers are well below the specified values, we can conclude that TPS6512x can reasonably power such a display.

SETTING THE OUTPUT VOLTAGE

The output voltages are defined as shown in Figure 22.

$$V_{MAIN} = V_{FBM} \times \frac{R5 + R6}{R6}$$

with an internal reference voltage V_{FBM} typical = 1.213V.

$$V_{GH} = V_{FBH} \times \frac{R1 + R2}{R2}$$

with an internal reference voltage V_{FBH} typical = 1.213V.

$$\left|V_{GL}\right| = V_{MAIN} \times \frac{R3}{R4}$$

To minimize the operating quiescent current, set R2, R4 and R6 in the range 100 kΩ to 300 kΩ. Great care should be taken to route the FBx lines away from noise sources such as the inductor or the SWN and SWP lines.

A feed-forward capacitor across the upper feedback resistor (R1, R3) on VGH and VGL outputs can be used to provide more overdrive for the error comparator. This feed-forward capacitor helps to reduce the output ripple voltage. A good starting value is 10 pF.

APPLICATION INFORMATION (continued)

The larger the feed-forward capacitor the worse the load regulation of the device. Therefore, when concern for load regulation is paramount, select a capacitor value as small as possible. Another possibility to further reduce ripple voltage on VGH and VGL outputs is to increase output-capacitor values (C2, C3).

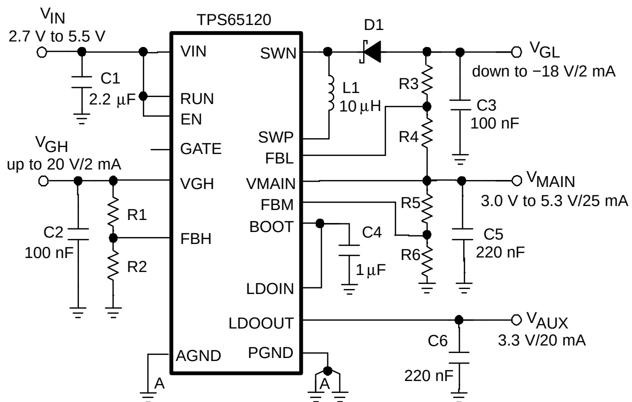


Figure 22. Typical Application

INDUCTOR SELECTION

Since the control scheme of the TPS6512x device is inherently stable, the inductor value does not affect the stability of the converter. To operate the TPS6512x properly at full performance, choose inductors in the range 8.2 µH to 10 µH.

The selection of the inductor is primarily based on the required output power. The variable peak current PWM control scheme used in TPS6512x automatically adapts the peak inductor current (between 65mA typ. and 150mA typ.) depending on output power and input voltage.

At moderate loads, the converter typically operates with a peak inductor current in the range of 65mA to 100mA, allowing the use of inductors in the 0603 case size. In order not to saturate the inductor when operating at a higher output power, select an inductor with a higher saturation-current rating.

The inductor series in Table 1 from various suppliers have been used with the TPS6512x converter.

Table 1. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
TAIYO YUDEN	LQ LB1608	1.6 x 0.8 x 0.8 = 1.02 mm^3
	LQ CB2012	2.0 x 1.2 x 1.2 = 2.88 mm^3
	LQ CBL2012	2.0 x 1.2 x 1.0 = 2.40 mm^3
TDK	GLF1608	1.6 x 0.8 x 0.8 = 1.02 mm^3
	GLF2012	2.0 x 1.2 x 1.2 = 2.88 mm^3

DIODE SELECTION

To achieve high efficiency, use a Schottky diode. The voltage rating must be higher than the input voltage plus the absolute value of the negative output. The current rating of the diode must meet the converter peak inductor-current rating when servicing the VGL output. The main parameter affecting the efficiency of the converter is the forward voltage and the reverse leakage current of the diode, both should be as low as possible.

The following diodes from different suppliers listed in Table 2 have been used with the TPS6512x converter.

Table 2. List of Diodes

MANUFACTURER	REFERENCE	REVERSE VOLTAGE
ROHM	RB521G-30	30 V
VISHAY	BAT54-HT3	30 V
ZETEX	ZUMD54	30 V

CAPACITOR SELECTION

The TPS65120 converter requires six capacitors. The input capacitor is primarily a function of the board layout. In designs with long traces, for good input filtering, we recommend a ceramic input capacitor (X5R/X7R type) of at least 1 µF placed as close as possible to the converter.

To operate properly, the TPS6512x requires a bootstrap capacitor of 1 µF (or larger) on the BOOT output. Additionally the minimum BOOT capacitance must be larger than two times the capacitor value connected to the MAIN and AUXILIARY LDO outputs (in case LDO AUX is connected to the BOOT output).

The TPS6512x peak-current control scheme is inherently stable. The filtering capacitors on VGH and VGL outputs are basically determined as a function of the required current and permissible ripple voltage. For small form-factor TFT-LCD applications, typical values in the range of 100 nF to 1 µF are usually required. A good starting point is 220 nF. For high output power on VGH and VGL outputs, the capacitance may need to approach 2 µF.

For stable operation, TPS6512x requires a 220-nF ceramic capacitor on the MAIN and AUXILIARY LDO outputs. Larger capacitor values can be used to achieve lower output-voltage noise without sacrificing stability.

In general, ceramic X5R types are strongly recommended for their low ESR and ESL and capacitance-versus-bias-voltage stability. Be certain that the capacitors used are rated for the maximum voltage with adequate safety margin.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. If the layout is not carefully done, the regulator could become unstable, displaying double or missing pulses as well as EMI problems. Therefore, use wide, short traces for the main current paths. Route these traces first.

Place the input capacitor as close as possible to the IC pins as well as the inductor and output capacitors. Place the inductor and diode as close as possible to the switch pins to minimize noise coupling into other circuits.

Use a common ground node for power ground and a different one for control ground (AGND) to minimize the effects of ground noise. Connect these ground nodes together (star point) at any place close to one of the ground pins of the IC and make sure that small-signal components returning to the AGND pin do not share the switching-current paths.

Feedback pins and divider networks are high-impedance nodes and should therefore be routed away from the inductor and shielded with a ground plane or trace to minimize noise coupling into the control loop.

APPLICATION EXAMPLES

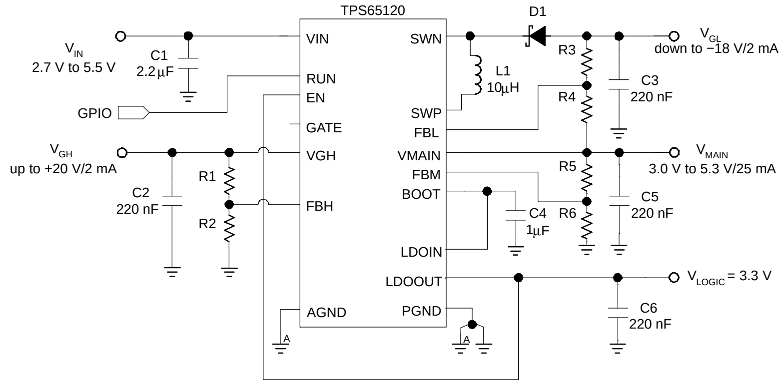
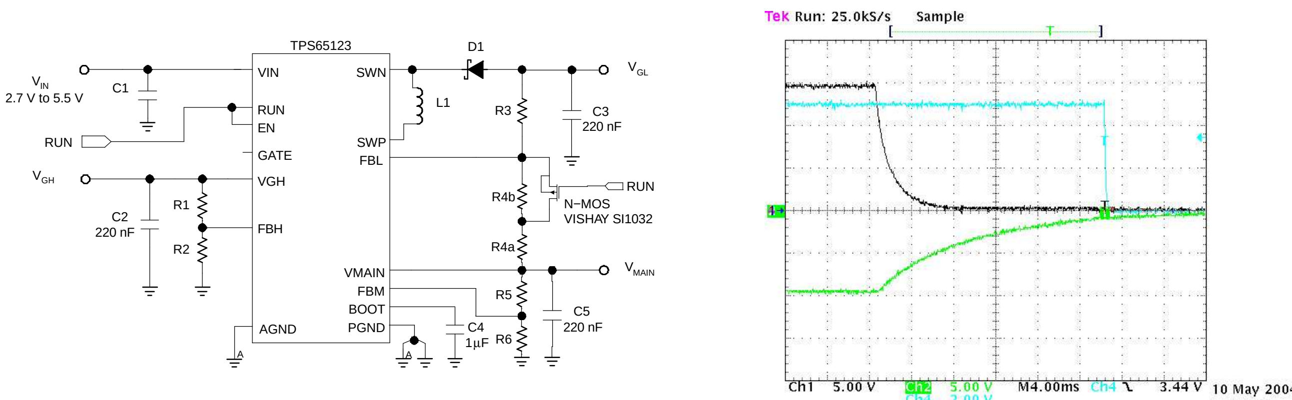


Figure 23. Complete TFT-LCD Power Supply from 1 cell Li-Ion

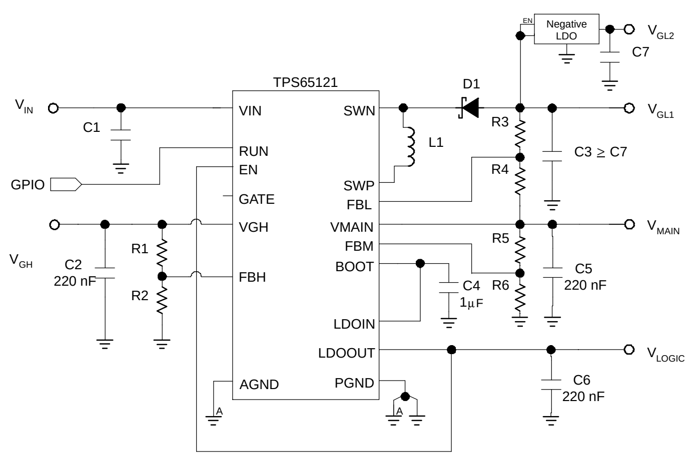


$$|V_{GL}| = V_{MAIN} \times \frac{R_3}{R_{4a}}$$

$$R_{4b} = R_3\left(\frac{1.2 - V_{MAIN}}{V_{GL\_OFFThreshold} - 1.2}\right) - R_{4a}$$

V_{MAIN} = 5.0 V, V_{GH} = 15 V, V_{GL} = −10 V
R_3 = 540 kΩ, R_{4a} = 270 kΩ, R_{4b} = 680 kΩ

Figure 24. $V_{GL} \rightarrow V_{MAIN}$ Power Down-Sequencing Threshold Shifting



Negative LDO = TPS723xx series

Figure 25. Additonal Negative Gate Driver Voltage

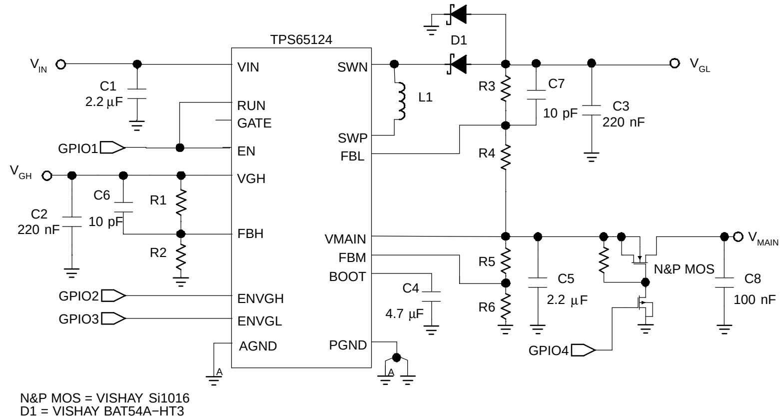


Figure 26. Fully Programmable Sequencing Featuring Very Low Gate Ripple Voltage

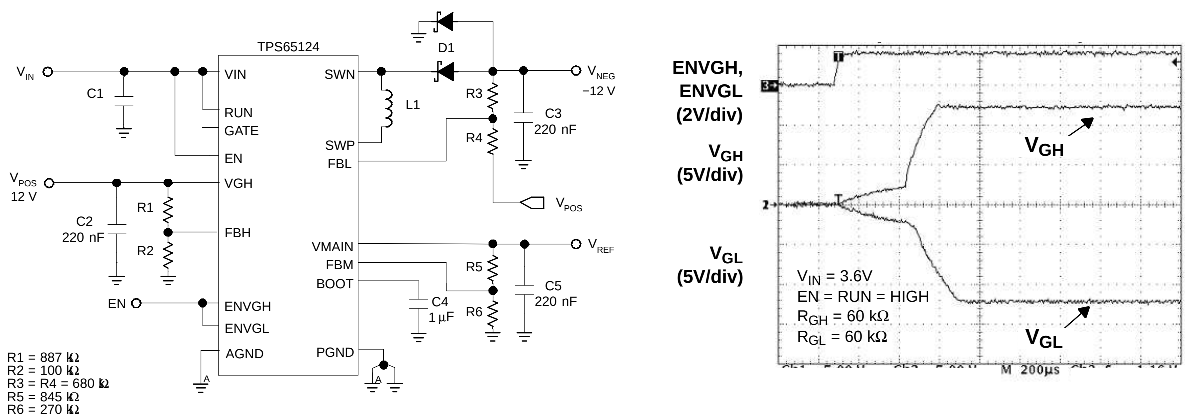


Figure 27. Dual Output Tracking Regulator with High Accuracy Reference Voltage

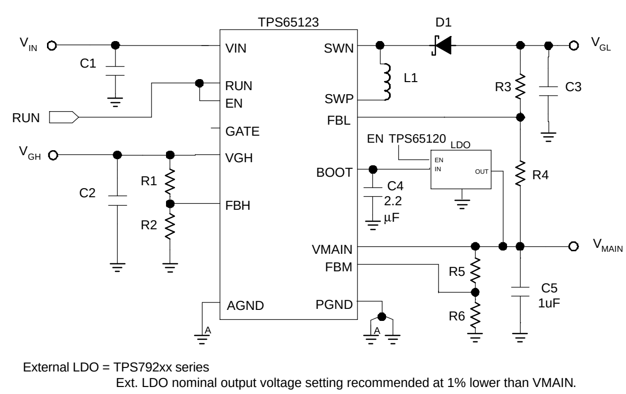


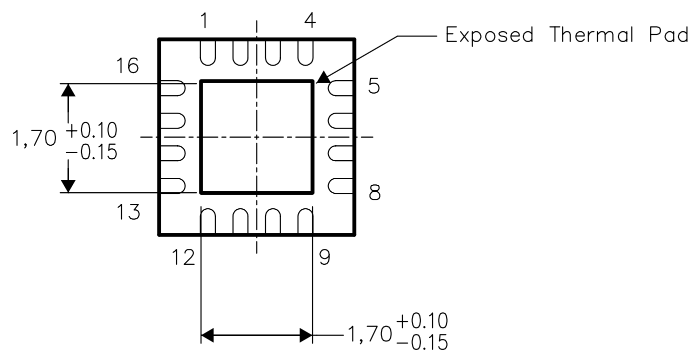
Figure 28. Boosting Main Output Current, I_{MAIN} > 25mA

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65120RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65120RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65120RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65120RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65121RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65121RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65121RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65121RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65123RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65123RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65123RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65123RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65124RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65124RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65124RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65124RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

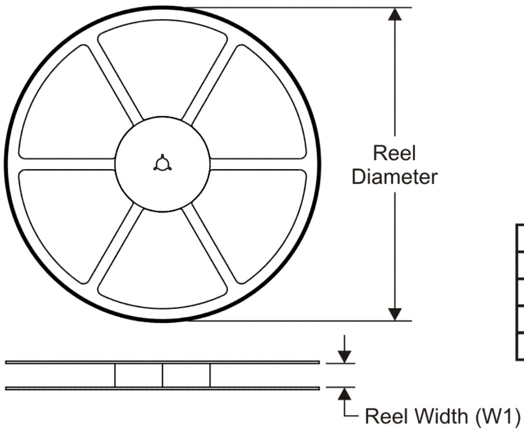
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

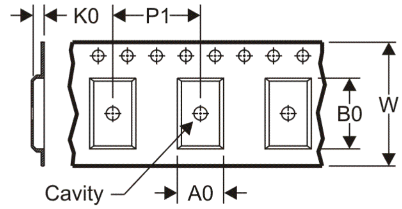
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

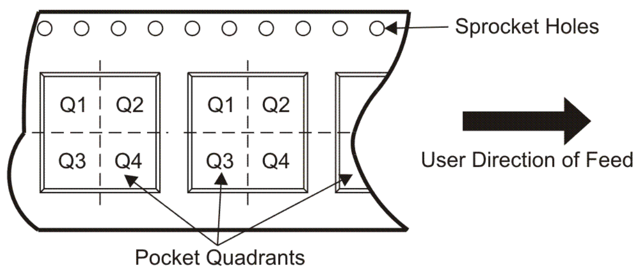


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

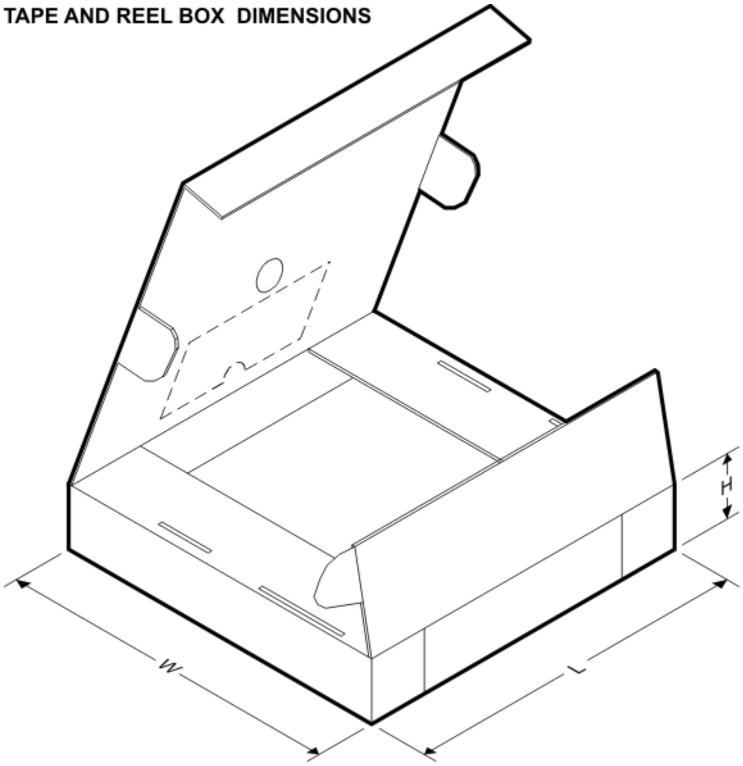
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65120RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65120RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65121RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65121RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65123RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65123RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65124RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65124RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

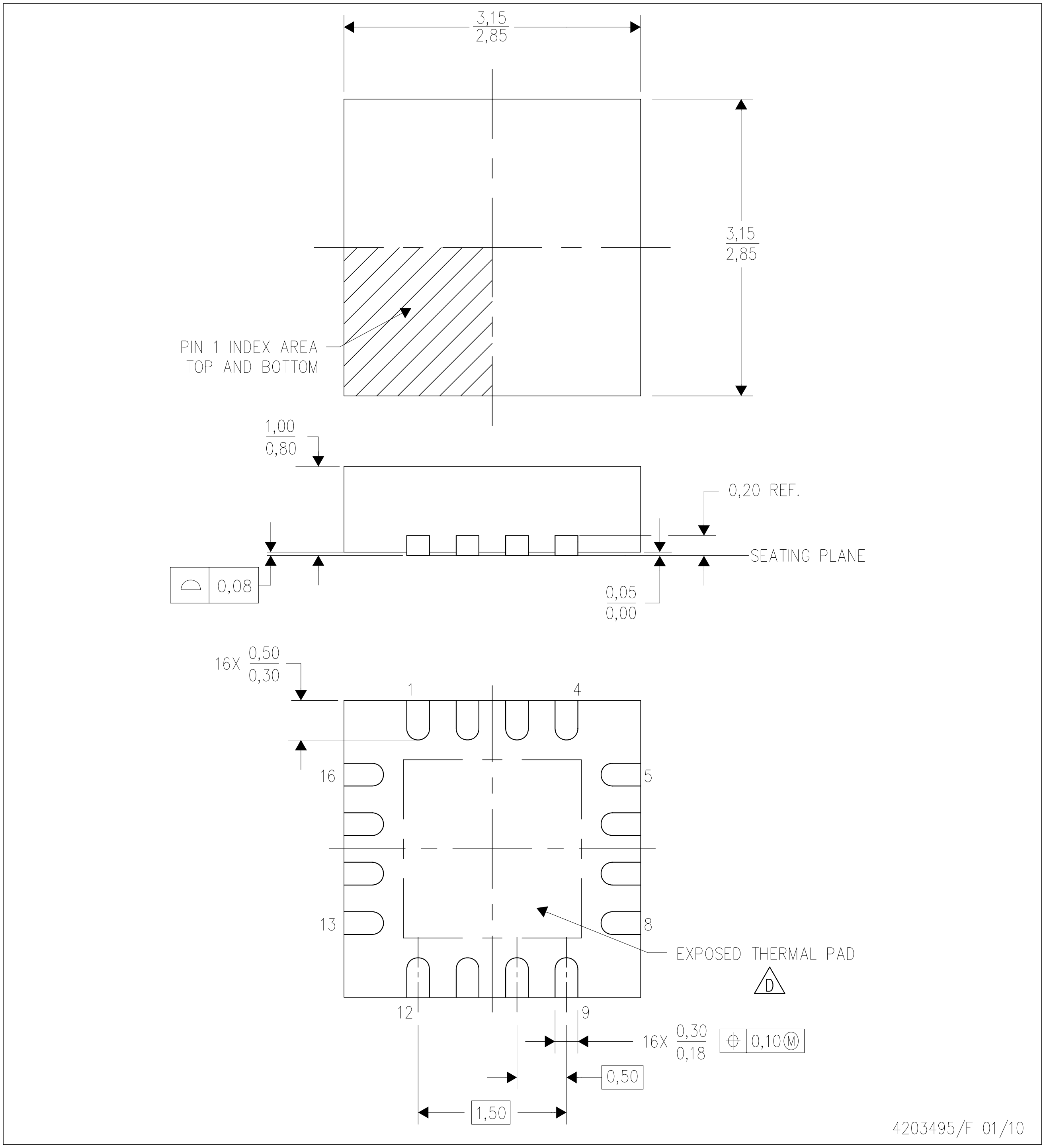
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65120RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
TPS65120RGTT	QFN	RGT	16	250	340.5	333.0	20.6
TPS65121RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
TPS65121RGTT	QFN	RGT	16	250	340.5	333.0	20.6
TPS65123RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
TPS65123RGTT	QFN	RGT	16	250	340.5	333.0	20.6
TPS65124RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
TPS65124RGTT	QFN	RGT	16	250	340.5	333.0	20.6

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



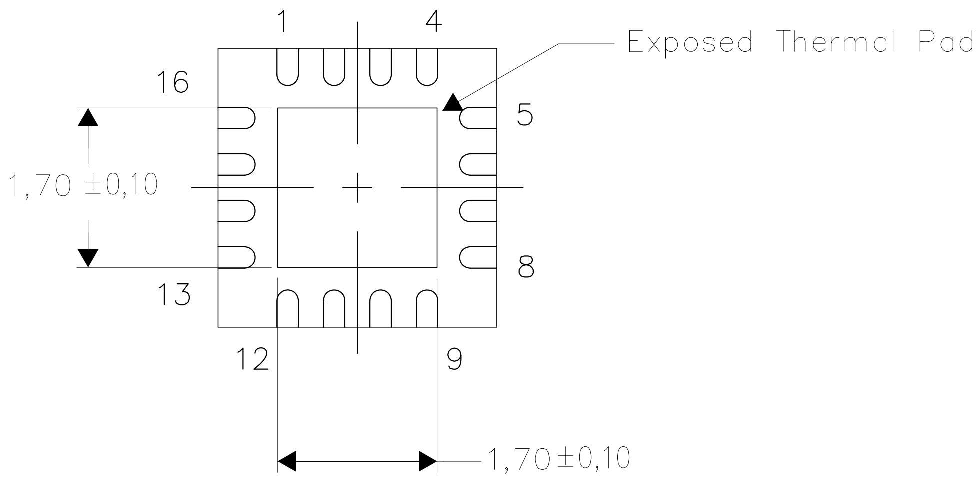
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

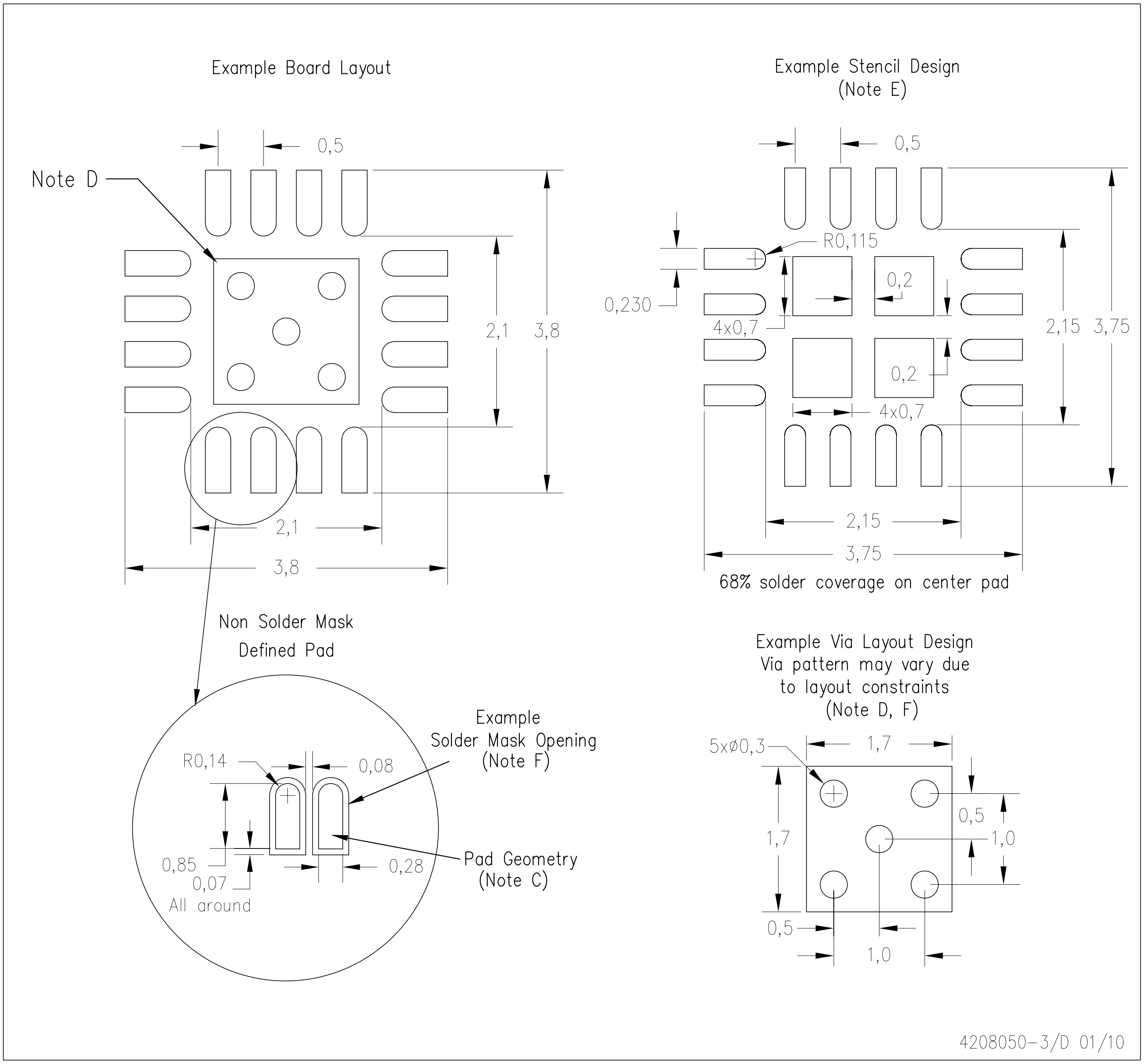


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S-PVQFN-N16)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.